In the claims:

Please amend the claims as follows:

1. (Currently amended) A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, said method comprising ~~the steps of~~:

simultaneously and selectively forming the oxide film on the floating gate of the ~~said~~ non-volatile memory cell transistor and a gate insulating film of the MOS transistor in a single thermal oxidation step.

2. (Cancelled)

3. (Currently amended) ~~A~~ The method of ~~manufacturing a semiconductor device according to~~ claim ~~2~~ 11, wherein said oxidation-resistant film is a silicon nitride film.

4. – 10. (Withdrawn)

11. (New) A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, said method comprising:

forming a silicon layer on the semiconductor substrate;

selectively removing the silicon layer on a region of the semiconductor substrate where the MOS transistor is to be formed;

forming an oxidation-resistant film over a first entire resulting surface;

selectively removing the oxidation-resistant layer on the region of the semiconductor substrate where the MOS transistor is to be formed and on a region of the semiconductor substrate where the floating gate of the non-volatile memory cell transistor is to be formed;

simultaneously and selectively forming an oxide film on the region where the floating gate is to be formed and a gate insulating film on the region where the MOS transistor is to be

formed; and

forming a tunneling insulating film over the gate insulating film.

12. (New) The method of claim 11 wherein the oxide film is formed by a single thermal oxidation step.

A1 Cont.

13. (New) A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on a same semiconductor substrate, said method comprising:

forming a first gate insulating film on the semiconductor substrate;

forming a silicon layer on the first gate insulating film;

selectively removing the silicon layer on a region of the semiconductor substrate where the MOS transistor is to be formed;

forming an oxidation-resistant film over a first entire resulting surface;

selectively removing the oxidation-resistant layer on the region of the semiconductor substrate where the MOS transistor is to be formed and on a region of the semiconductor substrate where the floating gate of the non-volatile memory cell transistor is to be formed;

simultaneously and selectively forming an oxide film on the region where the floating gate is to be formed and a second gate insulating film on the region where the MOS transistor is to be formed;

removing at least some of the remaining oxidation-resistant; and

forming a tunnel insulating film over a second entire resulting surface.

14. (New) The method of claim 13 wherein said oxidation-resistant layer is a silicon nitride layer.

15. (New) The method of claim 13 wherein the oxide film is formed by a single thermal oxidation step.

16. (New) The method of claim 13 further comprising selectively etching the tunnel insulating film on the region of the semiconductor substrate where the MOS transistor is to be formed.

17. (New) A semiconductor memory comprising:

a semiconductor substrate having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor formed on the semiconductor substrate,

wherein the oxide film on the floating gate of the non-volatile memory cell transistor and a gate insulating film of the MOS transistor are simultaneously and selectively formed in a single thermal oxidation step.

18. (New) An apparatus comprising:

a semiconductor memory having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor formed on a semiconductor substrate,

wherein the oxide film on the floating gate of the non-volatile memory cell transistor and a gate insulating film of the MOS transistor are simultaneously and selectively formed in a single thermal oxidation step.